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EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/649,437	Applicant(s) REYNOLDS ET AL.	
	Examiner Eduardo Garcia-Otero	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2000 and 16 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 August 2000* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: METHOD AND APPARATUS FOR SPECIFYING ADDRESSABILITY AND BUS CONNECTIONS IN A LOGIC DESIGN
2. First named inventor is: REYNOLDS
3. Claims 1-29 have been submitted, examined, and rejected.

Index

4. **Tabak** refers to Advanced Microprocessors, by Daniel Tabak, McGraw-Hill, Inc., ISBN: 0-07-062843-2, 1995.
5. **Microsoft Computer Dictionary** refers to Microsoft Computer Dictionary, Fourth Edition, by Microsoft Press, JoAnne Woodcock as Senior Contributor, ISBN 0-7356-0615-3, May 1999.
6. **McGraw-Hill Dictionary** refers to The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition, by McGraw-Hill Companies, Inc., ISBN 0-07-042313-X, 2003.

Filing date

7. The Examiner notes that the petition to correct filing date was granted, and that the correct filing date is 8/23/00.

Drawings-draftperson objection

8. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Specifically, see the enclosed Form 948, Notice of Draftperson's Drawing Patent Review which objects to the drawings.

Drawings-prior art

9. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

10. Specifically, specification page 4 line 6 states "Figure 1 is an exemplary logic diagram showing explicit addressability", and page 1 line 15 states "Traditional electronic design automation tool flows require the addressability and data connections of a device to a system bus to be explicitly specified".

Drawings-objections--reference characters

11. The drawings of this application improperly use reference characters. "The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts" according to 37 CFR 1.84(p)(4).

12. FIG 2, the lines/inputs SYMBOLIC, SIM, and BUSCLK do not have reference characters, and are not described in the appropriate part of the specification, pages 7 line 9 to page 8 line 10.

13. FIG 3, the lines/inputs SYMBOLIC, SIM, AWAIT, and BUSCLK do not have reference characters, and are not described in the appropriate part of the specification, page 8 lines 11-23. The line PHYSICAL does have a reference character, but is not discussed.

14. FIG 4 has similar difficulties, see specification page 8 line 24 to page 9 line 4.

Specification-objections

15. The Specification is objected to because of the following informalities. Appropriate correction is required.

16. The specification does not adequately describe the drawings; see drawing objections above.

Claim Rejections - 35 USC § 112- first paragraph- enablement

17. The following is a quotation of the first paragraph of 35 U.S.C. 112: The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

18. **Claims 1-29 are rejected under 35 U.S.C. 112, first paragraph,** as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

19. Claim 1 states **"data access primitive".** The specification does not adequately describe this term.

20. The most detailed description in the specification is for FIG 2. Specification page 7 line 9 to page 8 line 10 vaguely discusses the "exemplary diagram of a halfword selector data access primitive" of FIG 2. Three of the inputs are not discussed: SYMBOLIC, SIM, and BUSCLK. BUSCLK apparently refers to the bus clock, but the SYMBOLIC and SIM inputs are not clear.

21. Further, the specification page 7 line 4 broadly states "The logic designer uses a set of logic design components, referred herein as "data access primitives", to specify an assembly of address and lane-matching logic and associated data bus connections. The data access primitive **hides the details** of interconnection to the bus, and **abstracts away the**

interdependency of address-matching functions, lane-matching functions, and data bus connections." Emphasis added. Further, page 7 line 10 broadly states "Each data access primitive implies an address-matching function, one or more lane-matching functions, and bus connections for one or more bytes of data, as well as auxiliary logic."

22. The data access primitive of FIG 2 does hide the details and abstract away the interdependencies. Although it may be useful to hide the details and abstract away the interdependencies from the LSIC designer in order to ease his tedious burden, these very details and interdependencies must be disclosed in the specification for enablement. The Applicant is proposing to automate the "tedious" (page 1 line 23) specifying of addressibility and bus connections. Further, a 32-bit system bus is "much more complex... [with] interdependencies" (page 2 line 3), and no allowance for these interdependencies is disclosed in the specification.

23. Thus, claim 1 is not enabled.

24. Claims 2-29 are not enabled for the same reasons.

Claim Rejections - 35 USC § 112-Second Paragraph-indefinite claims

25. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

26. Claims 1-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

27. Claim 1 states **"data access primitive".** The specification does not adequately define this term. Note specification page 7 line 4 states "The logic designer uses a set of logic design

components, referred to herein as "data access primitives", to specify an assembly of address and lane-matching logic and associated data bus connections. The data access primitive hides the details of interconnection to the bus, and abstracts away the interdependency of address-matching functions, lane-matching functions, and data bus connections." Also see FIG 2 through FIG 5, which are described as primitives at specification page 4.

28. It is not clear if a "data access primitive" is hardware, or software, or merely an algorithm.

29. Note that Microsoft Computer Dictionary Fourth Edition defines "primitive" as "1. In computer graphics, a shape, such as a line, circle, curve, or polygon, that can be drawn, stored, manipulated as a discrete entity by a graphics program. A primitive is one of the elements from which a large graphic design is created. 2. In programming, a fundamental element in a language that can be used to create larger procedures that do the work a programmer wants to do". The second definition may apply.

30. The McGraw-Hill Dictionary of Scientific and Technical Terms, Sixth Edition defines "primitive" as "[COMPUT SCI] A sketchy specification, omitting details, of some action in a computer program. [CONT SYS] A basic operation of a robot, initialized by a single command statement in the program that controls the robot." **The first definition of McGraw-Hill ("sketchy specification") appears most appropriate.**

31. Thus, claim 1 is indefinite.

32. Claims 2-29 are indefinite for the same reasons.

Claim Interpretation

33. The claim language is interpreted in light of the specification. Limitations from the specification must not be imported into the claims, but definitions from the specification must be imported into the claims.

34. Claim 1, the Examiner hereby interprets **"data access primitive"** as not requiring the "other auxiliary logic" mentioned at specification page 1 line 18, and page 7 line 12. Note that "other auxiliary logic" is not mentioned in the limitations of claim 1, but rather appears to have been intentionally omitted.

35. Further, **"a data access primitive" is broadly interpreted to be a "sketchy specification"** according to the McGraw-Hill Dictionary, and may be either software, or hardware, or a mere algorithm.

36. Additionally, "a data access primitive" is interpreted as performing the same functions that traditionally are explicitly performed manually by the logic designers: see specification background page 1 lines 15-17, and see "specifying the addressability and bus connections may be tedious" at page 1 line 23.

37. These interpretations are consistently maintained throughout all the claims.

Claim Rejections - 35 USC § 102(b)

38. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

39. Claim 1-4, 6-13, 15-18, 20-24, and 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated.

40. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

41. Claim 1 is an independent method claim with 5 limitations.

42. A-**an address matching function** is disclosed by Tabak at page 48 "Address mapping".

43. B-**a lane matching function** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.

44. These microprocessors inherently lane match, because input data from the small external databus must be matched to the proper lane of the large internal databus. For example, in the 8088, during one clock cycle, 8 bits from the small external databus are placed in the first lane of the 16 bit large internal databus, and during the next clock cycle another 8 bits from the small external databus are placed in the second lane of the 16 bit large internal databus.

45. C-**one or more bus connections** is disclosed by Tabak at page 5 "internal databus" and "external databus".

46. D-**specifying a first starting address for the memory-mapped device** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping".

47. E-**generating a first set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device using the data access primitive and the first starting address** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.

48. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

49. Claim 2 depends from claim 1, with one additional limitation.

50. **generating a second set of addressing matching function, lane matching function and one or more bus connections for the memory-mapped device using the data access primitive and a second starting address** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.

51. Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

52. Claim 3 depends from claim 1, with two additional limitations.

53. A-**coupling the data access primitive to the memory-mapped device is** disclosed by

Tabak at Figure 4.4 "Cache-memory mapping".

54. B-**coupling an address bus to the data access primitive** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping".

55. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

56. Claim 4 depends from claim 3, with two additional limitations.

57. **the addressing matching function compares an address from the address bus with the first starting address for the memory-mapped device** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.

58. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

59. Claim 6 depends from claim 4, with one additional limitation.

60. **the first starting address is generated automatically** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.

61. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

62. Claim 7 depends from claim 6, with one additional limitation.

63. **the first starting address is generated automatically using a set of address constraints** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.

64. Claim 8 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

65. Claim 8 depends from claim 1, with one additional limitation.

66. **addressability for a minimum size transaction supported by the memory-mapped device** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.

67. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

68. Claim 9 depends from claim 8, with one additional

69. **the memory-mapped device is a register** is disclosed by Tabak at page 9 Figure 2.1

"Floating Point Register File (FRF)".

70. Claim 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.
71. Claims 10-13 are computer readable medium claims with the same limitations as method claims 1-4 respectively, and thus are rejected for the same reasons.
72. Claim 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.
73. Claims 15-17 are computer readable medium claims with the same limitations as method claims 6-8 respectively, and thus are rejected for the same reasons.
74. (Note that method claim 9 does not have a counterpart computer readable medium claim.)
75. Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.
76. Claim 18 is an independent method claim, with 7 limitations.
77. A-**an addressing matching function** is disclosed by Tabak at page 48 "Address mapping".
78. B- **lane matching function** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.
79. These microprocessors inherently lane match, because input data from the small external databus must be matched to the proper lane of the large internal databus. For example, in the 8088, during one clock cycle, 8 bits from the small external databus are placed in the first lane of the 16 bit large internal databus, and during the next clock cycle another 8 bits from the small external databus are placed in the second lane of the 16 bit large internal databus.
80. C-**one or more bus connections for a memory-mapped device** is disclosed by Tabak at page 5 "internal databus" and "external databus".
81. D-**specifying an address constraint for the memory-mapped device** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.
82. E-**generating a starting address for the memory mapped device using the address constraint** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at

page 11.

83. F-**generating the address matching function** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line 0 through Line k-1 of the Main Memory. Also see "memory management unit (MMU)" at page 11.

84. G-**generating the lane matching function** is disclosed by Tabak at page 4 Table 1.1. Note that the following Intel microprocessors have a small external databus and a large internal databus: 8088, 80188, 80376. The Examiner has taken the liberty of expanding Table 1.1 with the information from page 5 in order to make this point clear. The small external databus (half the size of the internal databus) is used to reduce costs associated with external processes, see Tabak page 5.

85. H-**the one or more bus connections** is disclosed by Tabak at page 5 "internal databus" and "external databus".

86. Claim 20 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

87. Claim 20 depends from claim 18, with one additional limitation.

the transaction size is one in a group comprising a byte, a halfword and a word is disclosed by Tabak at page 21 "byte", "halfword", and "word".

88. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

89. Claim 21 depends from claim 18, with one additional limitation.

90. **using a new starting address for the memory-mapped device without having to specify changes to the addressing function, the lane matching function and the one or more bus connections** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.

91. Claim 22 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

92. Claim 22 depends from claim 21, with one additional limitation.

93. **a different logic for the memory mapped device is instantiated automatically using the same data access primitive and the new starting address** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.

94. Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

95. Claim 23 depends from claim 18, with one additional limitation.

96. **the addressing matching function compares an address from an address bus coupled with the data access primitive with the starting address, and wherein when there is match, the lane matching function matching the transaction size of a transaction to a respective section of the memory-mapped device** is disclosed by Tabak at Figure 4.4 "Cache-memory mapping". See Line k through Line 2k of the Main Memory.

97. Claim 24 is rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

98. Claims 24 is computer readable medium claim with the same limitations as method claims 18, and thus is rejected for the same reasons.

99. Claim 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Tabak.

Claims 26-29 are computer readable medium claims with the same limitations as method claims 20-23 respectively, and thus are rejected for the same reasons.

Claim Rejections - 35 USC § 103

100. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject

matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

101. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- Determining the scope and contents of the prior art.
- Ascertaining the differences between the prior art and the claims at issue.
- Resolving the level of ordinary skill in the pertinent art.
- Considering objective evidence present in the application indicating obviousness or nonobviousness.

102. Claims 5, 14, 19, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable.

103. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabak in view of Applicant's Admission.

104. Claim 5 depends from claim 4, with one additional limitation.

105. Tabak does not explicitly disclose the additional limitation.

106. **the first starting address is specified by a user** is disclosed by Applicant's Admission at specification background page 1 line 23 "specifying the addressability and bus connections may be tedious", and page 2 lines 3-5 "interdependencies... make it much more likely that the logic designer will accidentally specify inconsistent addressability and bus connection information".

107. Regarding admissions, MPEP § 2129 states "When applicant states that something is prior art, it is taken as being available as prior art against the claims". *In re Nomiya*, 509 F.2d 566, 184 USPQ 607, 611 (CCPA 1975) states "admissions...may be considered "prior art" for any purpose, including use as evidence of obviousness under § 103". *Constant v. Advanced Micro-Devices,* 848 F2d 1560, 1570, 7 USPQ2d 1057, 1063 (Fed. Cir. 1988), "[Applicant's] own admission during prosecution...is binding upon him". Additionally, U.S. Patent and Trademark Office (USPTO), Formulating and Communicating Rejections Under 35 U.S.C. 1037 (Feb. 13, 1991) states when relying on an admission as evidence of obviousness, moreover, it is unnecessary to cite a corroborating reference to support the admission. Also see 37 C.F.R. § 1.104(c)(3).

108. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Applicant's Admission to modify Tabak. One of ordinary skill in the art would have been motivated to do this because it is required to "fully specify the addressability and bus connections of the memory-mapped devices" according to specification background page 1 line 11.

109. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabak in view of Applicant's Admission.

110. Claim 14 is a computer readable medium claim with the same limitations as method claim 5, and thus is rejected for the same reasons.

111. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabak in view of Applicant's Admission and *In re Venner* (legal precedent for making automatic).

112. Claim 19 depends from claim 18, with three additional limitations.

113. Tabak does not explicitly disclose the additional limitations.

114. A-**the address constraint is specified by a user** is disclosed by Applicant's Admission at specification background page 1 line 23 "specifying the addressability and bus connections may be tedious", and page 2 lines 3-5 "interdependencies... make it much more likely that the logic designer will accidentally specify inconsistent addressability and bus connection information".

115. B-**the starting address for the memory mapped device** is disclosed by Applicant's Admission at specification background page 1 line 23 "specifying the addressability and bus connections may be tedious", and page 2 lines 3-5 "interdependencies... make it much more likely that the logic designer will accidentally specify inconsistent addressability and bus connection information".

116. C-**[the starting address for the memory mapped device] is generated automatically** is disclosed by *In re Venner* (legal precedent for making automatic). *In re Venner,* 262 F.2d 91, 95, 120 USPQ 192, 194 (CCPA 1958) states "it is well settled that it is not "invention" to broadly provide a mechanical or automatic means to replace manual activity which has accomplished the same result." Additionally, MPEP 2144.04(III) states "broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art." Here, by Applicant's admission, at

specification background page 1 line 15-18 "Traditional electronic design automation tool flows require the addressability and data connections of a device to a system bus to be explicitly specified [by the designer]. This includes address matching, lane matching, connection to system bus data bits and any other auxiliary logic." Thus, generating the starting address automatically merely replaces "manual activity [by the designer] which has accomplished the same result".

117. **At the time** the invention was made, it would have been obvious to a person of ordinary skill in the art to use Applicant's Admission and *In re Venner* to modify Tabak. One of ordinary skill in the art would have been motivated to do this because it is required to "fully specify the addressability and bus connections of the memory-mapped devices" according to specification background page 1 line 11, and to save time and money and reduce errors by automating the addressability according to specification background page 1 line 23 "tedious" and page 2 line 5 "accidentally specify inconsistent addressability".

118. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tabak in view of Applicant's Admission and *In re Venner* (legal precedent for making automatic).

119. Claim 25 is a computer readable medium claim with the same limitations as method claim 19, and thus is rejected for the same reasons.

Additional Cited Prior Art

120. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action:

121. Virajpet US Patent 6,480,948 B1 column 1 line 9 discloses "a memory map may be created which reflects the addressabilityof devices coupled together in a system".

122. Heffron US Patent 5,438,509 Column 4 line 50 discloses "data access primitive".

123. Helbig US Patent 5,278,847 Column 2 line 40 disclosed "memory map".

Communication

124. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 7:00 PM.

125. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone numbers for this group are:

126. (703) 746-7238 --- for communications after a Final Rejection has been made;

127. (703) 746-7239 --- for other official communications; and

128. (703) 746-7240 --- for non-official or draft communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

* * *

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100